

**What is claimed is:**

- 1    1.    An article comprising:  
2            a first peak detector to generate an output in response to detection of a peak  
3    amplitude of a received signal at an input terminal;  
4            a first amplifier to compare the peak amplitude and a first reference potential  
5    and generate a feedback signal coupled through a resistance to the input terminal;  
6    and  
7            a second amplifier to compare the received signal and a second reference  
8    potential.
- 1    2.    The article of claim 1 further including a maximum level detector and a  
2    minimum level detector, each having an output coupled by a voltage divider to  
3    provide the first reference potential.
- 1    3.    The article of claim 1 further including a capacitor coupled to the input  
2    terminal to provide isolation.
- 1    4.    The article of claim 1 wherein the first peak detector includes a maximum  
2    high level peak detector.
- 1    5.    The article of claim 1 wherein the first peak detector includes a minimum  
2    low level peak detector.
- 1    6.    The article of claim 1 wherein the resistance includes a transistor.
- 1    7.    The article of claim 1 further including a filter coupled to the first amplifier.
- 1    8.    A circuit comprising:  
2            a feedback amplifier having a feedback output and a first feedback input and  
3    having a second feedback input to couple with a first reference potential;

4           a peak detector having a detector output coupled to the first feedback input  
5   and having a detector input;  
6           a feedback circuit coupled to the feedback output and coupled to the detector  
7   input; and  
8           a receiver amplifier having a first receiver input coupled to the detector input  
9   and having a second receiver input adapted to couple with a second reference  
10   potential.

1   9.     The circuit of claim 8 wherein the feedback circuit includes a resistor.

1   10.    The circuit of claim 8 wherein the feedback circuit includes a transistor.

1   11.    The circuit of claim 8 further including a filter coupled between the first  
2   feedback input and the feedback output.

1   12.    A system comprising:  
2           a driver having a primary output terminal;  
3           a receiver having a primary input terminal coupled to the primary output  
4   terminal;  
5           a primary peak detector coupled to the primary input terminal and having a  
6   primary peak output;  
7           an output amplifier having a first amplifier input coupled to the primary  
8   input terminal and a second amplifier input coupled to a first reference potential;  
9           a primary feedback amplifier having a first primary feedback input coupled  
10   to the primary peak output and a second primary feedback input coupled to a second  
11   reference potential and having a primary feedback output; and  
12           a primary feedback circuit coupled to the primary feedback output and  
13   coupled to the primary input terminal.

1   13.    The system of claim 12 further including a capacitor between the primary  
2   output terminal and the primary input terminal.

1 14. The system of claim 12 further including a primary filter coupled between  
2 the first primary feedback input and the primary feedback output.

1 15. The system of claim 14 wherein the primary filter includes a capacitor.

1 16. The system of claim 12 wherein the primary feedback circuit includes a  
2 resistor.

1 17. The system of claim 12 wherein the primary feedback circuit includes a  
2 transistor.

1 18. The system of claim 12 wherein the primary input terminal is coupled to the  
2 primary output terminal by a cable.

1 19. The system of claim 12 wherein the primary input terminal is coupled to the  
2 primary external output terminal by a backplane.

1 20. The system of claim 12 wherein the driver includes a secondary output  
2 terminal and the receiver includes a secondary input terminal coupled to the  
3 secondary output terminal and further including:  
4 a secondary peak detector coupled to the secondary input terminal and  
5 having a secondary peak output;  
6 a secondary feedback amplifier having a first secondary feedback input  
7 coupled to the secondary peak output and a second secondary feedback input  
8 coupled to the primary peak output and having a secondary feedback output; and  
9 a secondary feedback circuit coupled to the secondary feedback output and  
10 coupled to the secondary input terminal; and  
11 wherein the second amplifier input is coupled to the secondary input  
12 terminal.

1 21. A method comprising:  
2 detecting a peak amplitude of an input signal;  
3 generating a feedback signal as a function of a comparison of the peak  
4 amplitude and a first reference potential;  
5 biasing the input signal with the feedback signal; and  
6 generating an output signal as a function of a comparison of the input signal  
7 and a second reference potential.

1 22. The method of claim 21 wherein detecting the peak includes detecting a  
2 peak high value.

1 23. The method of claim 21 wherein generating the feedback signal includes  
2 generating an amplified signal based on a differential between the peak and the first  
3 reference level.

1 24. The method of claim 21 wherein detecting the peak in the input signal  
2 includes receiving the input signal from a signal source and further including  
3 receiving the second reference potential from the signal source.

1 25. The method of claim 21 further including generating the second reference  
2 potential by averaging a maximum high value of the input signal and a minimum  
3 low value of the input signal.

1 26. A method comprising:  
2 receiving a first reference potential;  
3 sampling an input signal relative to the first reference potential;  
4 generating a correction signal based on a peak amplitude in the sampled  
5 input signal; and  
6 biasing the input signal as a function of the correction signal.

1 27. The method of claim 26 wherein receiving the first reference potential  
2 includes generating the first reference potential as a function of a maximum high  
3 value of the input signal and a minimum low value of the input signal.

1 28. The method of claim 26 wherein generating the correction signal based on  
2 the peak amplitude in the sampled input signal includes detecting the maximum  
3 high value in the sampled input signal.

1 29. The method of claim 26 wherein biasing includes generating a differential  
2 amplified signal based on a comparison of the peak amplitude and a second  
3 reference potential.

1 30. A method comprising:  
2 sampling a pair of complementary input signals;  
3 generating a pair of complementary correction signals, each correction signal  
4 based on a peak amplitude in an input signal of the pair of complementary input  
5 signals; and  
6 biasing each input signal of the complementary input signals as a function of  
7 the correction signals.

1 31. The method of claim 30 wherein generating the pair of complementary  
2 correction signals includes generating an amplified differential signal.

1 32. The method of claim 30 further including generating an output signal as a  
2 function of each input signal of the complementary input signals.

1 33. A system comprising:  
2 a reduced instruction set computer having an output terminal;  
3 a first peak detector having an input terminal coupled to the output terminal  
4 and to generate an output in response to detection of a peak amplitude of a received  
5 signal at the input terminal;

6           a first amplifier to compare the peak amplitude and a first reference potential  
7   and generate a feedback signal coupled through a resistance to the input terminal;  
8   and  
9           a second amplifier to compare the received signal and a second reference  
10   potential.

1   34.    The system of claim 33 wherein the reduced instruction set computer  
2   provides an output signal having an unbalanced duty cycle.

1   35.    The system of claim 33 wherein the reduced instruction set computer  
2   provides a single ended signal.